wherein the bottom surface is provided with electrical connections adapted to be connected to a substrate.

2. The windowframe capacitor of Claim 1, wherein the aperture is rectangular.

3. The windowframe capacitor of Claim 1, wherein the capacitive material comprises a layer of an electrically conductive material and a layer of a dielectric material.

4. The windowframe capacitor of Claim 3, wherein the housing is made from a plastic material.

5. The windowframe capacitor of Claim 1, wherein said electrical connections provided on the bottom surface comprise a ball grid array.

6. The windowframe capacitor of Claim 1, wherein the capacitive material and the housing comprise co-fired ceramic.

7. The windowframe capacitor of Claim 1, wherein the aperture is configured to fit over a semiconductor die, and wherein said electrical connections are configured for connection to a package substrate on which the semiconductor die is mounted.

8. A semiconductor package assembly, comprising:

a semiconductor die mounted on a portion of a top surface of a package substrate; and

a windowframe capacitor having an aperture formed therein, and mounted on the top surface of the package substrate surrounding the semiconductor die.

9. The semiconductor package assembly of Claim 8, further comprising an electronic component mounted on a top surface of the windowframe capacitor.

10. The semiconductor package assembly of Claim 8, further comprising a second windowframe capacitor mounted on a top surface of the first windowframe

capacitor.

11. The semiconductor package assembly of Claim 8, wherein the aperture is rectangular.

12. The semiconductor package assembly of Claim 8, wherein the windowframe capacitor comprises a housing.

13. The semiconductor package assembly of Claim 12, wherein the windowframe capacitor comprises a capacitive material disposed within the housing.

14. The semiconductor package assembly of Claim 13, wherein the capacitive material comprises a layer of an electrically conductive material and a layer of a dielectric material.

15. The semiconductor package assembly of Claim 14, wherein the housing is made of a plastic material.

16. The semiconductor package assembly of Claim 13, wherein the capacitive material and the housing comprise a co-fired ceramic.

17. The semiconductor package assembly of Claim 8, wherein the windowframe capacitor is mounted on the package substrate via a ball grid array.

REMARKS

Please reconsider the application in view of the above amendments and the following remarks.

I. Specification

The Examiner objected to the Specification because the advantages of the invention were not disclosed in the "Brief Summary of the Invention" section of the Specification. In response, Applicant has amended the Specification such that the advantages of the invention are

now disclosed in the "Brief Summary of the Invention" section of the Specification. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in original (now deleted) paragraph [0022] of the Specification. Accordingly, favorable entry of this amendment is respectfully requested.

II. Drawings

The Examiner objected to the drawings under 37 C.F.R. 1.83(a) as not showing every feature of the invention as specified in the claims. Specifically, the Examiner stated that the 'housing having an aperture' feature recited in claim 1 is not shown. However, Figure 4 of the present application does show such a feature. In Figure 4, the housing, i.e., the windowframe capacitor **27**, is shown with an aperture, or opening, through which the semiconductor die **11** is positioned. Thus, the 'housing having an aperture' feature is shown, and accordingly, withdrawal of the objection to the drawings is respectfully requested.

III. Objections to the Claims

The Examiner objected to the numbering style of claims 1-17. Accordingly, Applicant has amended claims 1-17 to address these informalities, and withdrawal of the objections to claims 1-17 is respectfully requested. No new matter has been added by way of these amendments.

IV. Disposition of the Claims

Claims 1-17 are pending in the present application. Claims 1-17 have been amended.

V. Rejection(s) Under 35 U.S.C. § 112

The Examiner rejected claims 1-7 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner stated that it is not clear what is meant by the "an aperture is formed in a central portion" language in claim 1. As shown in Figure 4 of the present application, the windowframe capacitor **27** is configured so as to surround semiconductor die **11**. *See also* Specification, paragraph [0018]. Thus, the windowframe capacitor **27**, as shown in Figure 4 of the present application, is designed to have an aperture, or

opening, in a central portion so as to allow the windowframe capacitor **27** to surround the semiconductor die **11**. Moreover, for purposes of clarity, Applicant has amended the "an aperture is formed in a central portion" language in claim 1 to "an aperture in a central portion." Accordingly, for the reasons stated above, withdrawal of the § 112 rejection is respectfully requested.

VI. Rejection(s) Under 35 U.S.C. § 102

The Examiner rejected claims 1, 2, 5, and 7 were rejected under 35 U.S.C. § 102 as being anticipated by Applicant's Prior Art figures. For the reasons set forth below, the rejection is respectfully traversed.

The present invention relates to a capacitor that is generally configured in the shape of a windowframe, and hence referred to as "windowframe capacitor." Specification, paragraph [0018]. As shown in Figure 4 of the present application, such a configuration allows the windowframe capacitor to be positioned around a semiconductor die on a chip package substrate. Moreover, such a capacitor design allows for an increase in effective capacitance while decreasing high inductances normally associated with a multitude of individual high frequency capacitors. Accordingly, claim 1 of the present application requires at least that a capacitor have an aperture, or opening, in a central portion thereof.

Applicant's Prior Art figures fail to disclose this element. For example, Prior Art Figure 2 of the present application simply shows multiple capacitors **17** positioned on a chip package substrate **13**. None of the capacitors in Applicant's Prior Art figures show "an aperture" as recited in amended claim 1. Thus, Applicant's Prior Art figures fail to either inherently or explicitly disclose a capacitor having an aperture. Advantageously, embodiments of the invention allow the capacitor to surround a semiconductor die on a chip package substrate (see, e.g., Figure 4 of the present application). Accordingly, Applicant's Prior Art figures fail to anticipate the claims of the present application, and withdrawal of the § 102 rejection is respectfully requested. Claims 2, 5, and 7, which depend from amended claim 1, are patentable for at least the same reasons.

VII. Rejection(s) Under 35 U.S.C. § 103

The Examiner rejected claim 3 under 35 U.S.C. § 103(a) as obvious over Applicant's Prior Art figures in view of U.S. Patent No. 6,072,211 issued to Miller et al. (hereinafter "Miller"). As shown in Figure 1 of Miller, Miller is directed to a semiconductor package **10** that uses an insulator **12** to form a shunt capacitor. Miller is completely silent with regard to a capacitor having an aperture as recited in amended claim 1. Thus, Miller fails to disclose the limitations of amended claim 1 that are not disclosed by Applicant's Prior Art Figures. Accordingly, Applicant's Prior Art figures or Miller, whether considered in combination or alone, cannot render claim 3 obvious, and withdrawal of the § 103 rejection of claim 3 is respectfully requested.

The Examiner rejected claims 4 and 6 under 35 U.S.C. § 103(a) as obvious over Applicant's Prior Art figures in view of Miller and U.S. Publication No. 2002/0011354 (hereinafter "Barnett"). Barnett is directed to low temperature co-fired ceramic multichip modules that are used to provide high density interconnects between electric elements. Barnett, Abstract. Barnett is completely silent as to a capacitor that has an aperture so as to allow the capacitor to surround a semiconductor die on a chip package substrate. Thus, Barnett fails to disclose the limitations of amended claim 1 that are not disclosed by Applicant's Prior Art Figures or Miller. Accordingly, Applicant's Prior Art figures, Miller, or Barnett, whether considered in any combination or alone, cannot render claims 4 and 6 obvious, and withdrawal of the § 103 rejections of claims 4 and 6 is respectfully requested.

VIII. Allowed Claims

The Examiner allowed claims 8-17. Applicant thanks Examiner for reviewing and allowing claims 8-17.

IX. Conclusion

The claims have been shown to be allowable over the prior art. Applicant believes that this paper is responsive to each and every ground of rejection cited by the Examiner in the Action dated December 3, 2002 and respectfully requests favorable action in the form of a Notice of Allowance.

Please apply any charges not covered, or any credits, to Deposit Account 50-0591

(Reference Number 03226.092001/P5787).

Respectfully submitted,

Date: 1/17/03

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